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EXAMINER

KOLAHDOUZAN, HAJAR

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/587,237	Applicant(s) ARAI ET AL.	
	Examiner HAJAR KOLAHDOUZAN	Art Unit 2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 July 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 July 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/19/2010 has been entered.

Response to Arguments

Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 2- 6, and 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al (US 2003/0034497 A1).

Regarding claim 2, Yamazaki [Figs.1-2B, Fig.6B] teaches a semiconductor device comprising:

an integrated circuit using a thin film transistor [104a-c/303a-c];

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an antenna [the upper conductive bar that is connected to the TFT 104c/303c]; a first sealing film [114/307];

a second sealing film [111/306]; a substrate [112/302]; a first adhesive [113/308], a second adhesive [305] and a cover member [110/301],

wherein the integrated circuit [104/303] and the antenna [the upper conductive bar that is connected to the TFT 104c/303c] are electrically connected to each other [shown],

the integrated circuit [104/303] is sandwiched between the first sealing film [114/307] and the second sealing film [111/306],

the first sealing film [114/307] and the second sealing film [111/306] are sandwiched between the substrate [112/302] and the cover member [110/301],

the first sealing film [114/307] is attached to the substrate [112/302] with the first adhesive [113/308] is a bonding layer that sticks the substrate and sealing film together as shown in fig.2B and 6B],

the first sealing film [114/307] includes a plurality of first insulating films [114a/307a and 114c/307c] and one or a plurality of second insulating films [114b/307b] sandwiched between the plurality of first insulating films [shown],

the second sealing film [111/306] includes a plurality of third insulating films [111a/306a and 111c/306c] and one or a plurality of fourth insulating films [111b/306b] sandwiched between the plurality of third insulating films [shown],

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the one or the plurality of second insulating films [114b/307b] has lower stress than the plurality of first insulating films [114b/307b is a stress relaxing layer],

the one or the plurality of fourth insulating films [111b/306b] has lower stress than the plurality of third insulating films [111b/306b is a stress relaxing layer],

the plurality of first insulating films and the plurality of third insulating films are inorganic insulating films;

the integrated circuit [303] provided over the substrate [302] is covered with the second adhesive [305],

the second adhesive [305] is in contact with the second sealing film [306], and

the second adhesive [305] is partly in contact with the substrate [302] over which the first adhesive [308], the first sealing film [307], and the integrated circuit are provided [303, it is shown in fig.6B that all the layers and films are contacting each other and to the substrate]

Regarding claim 3, Yamazaki [figs. 1-2B and fig.6B] teaches a semiconductor device comprising:

an integrated circuit using a thin film transistor [104]; an antenna [the upper conductive bar that is connected to the TFT 104c/303c];

a first sealing film [114/307]; a second sealing film [111/306]; a substrate [112/302]; a first adhesive [113/308]; a second adhesive [305]; and a cover member [110/301],

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wherein the integrated circuit [104/303] and the antenna [the upper conductive bar that is connected to the TFT 104c/303c] are electrically connected to each other [shown],

the integrated circuit [104/303] and the antenna [the upper conductive bar that is connected to the TFT 104c/303c] are sandwiched between the first sealing film [114/307] and the second sealing film [111/306],

the first sealing film [114] and the second sealing film [111] are sandwiched between [shown] the substrate [112] and the cover member [110],

the first sealing film [114/307] is attached to the substrate [112/302] with the first adhesive [113/308 is a bonding layer that sticks the substrate and sealing film together as shown in fig.2B and 6B],

the first sealing film [114] includes a plurality of first insulating films [114a and 114c] and one or a plurality of second insulating films [114b] sandwiched between the plurality of first insulating films [it is shown that the layer 114b is sandwiched between 114a and 114c],

the second sealing film [111] includes a plurality of third insulating films [111a and 111c] and one or a plurality of fourth insulating films [111b] sandwiched between the plurality of third insulating films [it is shown that layer 111b is sandwiched between 111a and 111c],

the one or the plurality of second insulating films [114b] has lower stress than the plurality of first insulating films [114 is a stress relaxing layer],

the one or the plurality of fourth insulating films [111b] has lower stress than the plurality of third insulating films [111b is a stress relaxing layer],

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the plurality of first insulating films [114a and 114c (barrier layers)] and the plurality of third insulating films [111a and 111c (barrier layers)] are inorganic insulating films [paragraph 0017],

the integrated circuit [104/303] and the antenna [the upper conductive bar that is connected to the TFT 104c/303c] provided over the substrate [112/302] are covered with the second adhesive [305],

the second adhesive [305] is in contact with the second sealing film [306], and

the second adhesive [305] is partly in contact with the substrate [302] over which the first adhesive [308], the first sealing film [307], the integrated circuit [303], and the antenna [[the upper conductive bar that is connected to the TFT 104c/303c] are provided.

Regarding claim 4, Yamazaki [paragraph 0077] teaches that the cover member [110] has flexibility.

Regarding claim 5, Yamazaki [Fig.1-2 and 6] teaches that the antenna [the upper conductive bar that is connected to the TFT 104c/303c] and a gate electrode of the thin film transistor are formed using a conductive film [paragraph 0240 and 0224-0225].

Regarding claim 6, Yamazaki [Fig.1-2 and 6] teaches that the antenna [the upper conductive bar that is connected to the TFT 104c/303c] and a wiring connected to the thin film transistor are formed using a conductive film [paragraph 0224-0226].

Regarding claim 10, Yamazaki [paragraph 0077] teaches that the substrate [112] has flexibility.

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Regarding claim 11, Yamazaki [paragraph 0070] teaches that the plurality of first insulating films [114a and 114c] or the plurality of third insulating films [111a and 111c] includes silicon nitride, silicon nitride oxide, aluminum oxide, aluminum nitride, aluminum nitride oxide or aluminum silicon nitride oxide.

Regarding claim 12, Yamazaki [paragraph 0072] teaches that the one or the plurality of second insulating films [114b] or the one or the plurality of forth insulating films [111b] includes polyimide, acrylic, polyamide, polyimide amide, benzocyclobutene or epoxy resin.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Yamazaki (20010040645) hereinafter Yamazaki645.

Regarding claim 1, Yamazaki [figs.1-2B] teaches a semiconductor device comprising:

- an integrated circuit using a thin film transistor [104a-c];
- an antenna [the upper conductive bar that is connected to the TFT 104c; the broadest reasonable definition of an antenna is a “usually metallic device (as a rod or wire)”. The bar that applicant also point to it by the upper arrow is a conductive bar which can receive or radiate waves of any kind];

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a first sealing film [114]; a second sealing film [111]; a protective layer [108]; a substrate [112]; and an adhesive [113],

wherein the integrated circuit [104] and the antenna [the upper conductive bar that is connected to the TFT 104c] are electrically connected to each other [shown],

the antenna [the upper conductive bar that is connected to the TFT 104c] is covered with the protective layer [108, shown in figs.1-2];

the integrated circuit [104] is sandwiched between [shown in fig.2B] the first sealing film [114] and the second sealing film [111],

the first sealing film [114] is sandwiched between the substrate [112] and the integrated circuit [104],

the first sealing film [114/307] is attached to the substrate [112/302] with the adhesive [113/308 is a bonding layer that sticks the substrate and sealing film together as shown in fig.2B and 6B],

the first sealing film [114] includes a plurality of first insulating films [114a and 114c] and one or a plurality of second insulating films [114b] sandwiched between the plurality of first insulating films [shown],

the second sealing film [111] includes a plurality of third insulating films [111a and 111c] and one or a plurality of fourth insulating films [114b] sandwiched between the plurality of third insulating films [shown in fig.1C],

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the one or the plurality of second insulating films [114b] has lower stress than the plurality of first insulating films [114b is a stress relaxing layer],

the one or the plurality of fourth insulating films [111b] has lower stress than the plurality of third insulating films [111b is a stress relaxing layer],

the plurality of first insulating films [114a and 114c (the barrier layers)] and the plurality of third insulating films [111a and 111c (the barrier layers)] are inorganic insulating films [paragraph 0017],

the adhesive [103] over the substrate [112], the integrated circuit [104a-c] over the first sealing film [103], the antenna [the upper conductive bar that is connected to the TFT 104c] over the integrated circuit [104a-c], and the protective layer [108] over the antenna [the upper conductive bar that is connected to the TFT 104c] are covered with the second sealing film [111], and the second sealing film is partly in contact with the substrate [it is shown in the figure that all the layers are contacting each other].

Yamazaki however does not disclose that the first sealing film is over the adhesive.

Yamazaki645 [Fig.1] teaches a substrate [11] and an adhesive layer [58] on the substrate and attaching a sealing film [12] to the substrate by using the adhesive [58] in between. It also teaches having an integrated circuit [TFT, 201].

It is well known in the art to use an adhesive to attach or connect a substrate to any layer including a sealing film.

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Therefore it would have been obvious to one ordinary skill in the art at the time of the invention to use an adhesive to attach or connect a substrate to any layer including a sealing film because an adhesive would ensure a better attachment or connection between the two surface and semiconductor structure as a whole would be more reliable having lower chance of breakage or damage.

Regarding claim 10, Yamazaki in view Yamazaki645 was discussed in claim 1.

Yamazaki [paragraph 0077] teaches that the substrate [112] has flexibility.

Regarding claim 11, Yamazaki in view Yamazaki645 was discussed in claim 1.

Yamazaki [paragraph 0070] teaches that the plurality of first insulating films [114a and 114c] or the plurality of third insulating films [111a and 111c] includes silicon nitride, silicon nitride oxide, aluminum oxide, aluminum nitride, aluminum nitride oxide or aluminum silicon nitride oxide.

Regarding claim 12, Yamazaki in view Yamazaki645 was discussed in claim 1.

Yamazaki [paragraph 0072] teaches that the one or the plurality of second insulating films [114b] or the one or the plurality of forth insulating films [111b] includes polyimide, acrylic, polyamide, polyimide amide, benzocyclobutene or epoxy resin.

Claims 7-8 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Yamazaki et al. [hereinafter Yamazaki2] (US 2002/0134979 A1) in view of Moon et al. (US 6,844,906).

Regarding claim 7, Yamazaki [figs.1-2B and fig.6B] teaches a semiconductor device comprising:

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an integrated circuit using a thin film transistor [104a-c/303a-c]; an antenna [the upper conductive bar that is connected to the TFT 104c/303c]; a first sealing film [114/307]; a second sealing film [111/306]; a substrate [112/302]; a first adhesive [113/308]; a second adhesive [305]; and a cover member [110],

wherein the integrated circuit [104/303] is sandwiched between the first sealing film [114/307] and the second sealing film [111/306],

the first sealing film [114/307] and the second sealing film [111/306] are sandwiched between [shown] the substrate [112/302] and the cover member [110],

the first sealing film [113/308] is attached to the substrate [112/302] with the first adhesive [113/308];

the first sealing film [114/307] includes a plurality of first insulating films [114a/303a and 114c/303c] and one or a plurality of second insulating films [114b/303b] sandwiched between the plurality of first insulating films [shown],

the second sealing film [111/306] includes a plurality of third insulating films [111a/303a and 111c/303c] and one or a plurality of fourth insulating films [111b/303b] sandwiched between the plurality of third insulating films [shown],

the one or the plurality of second insulating films [114b/306b] has lower stress than the plurality of first insulating films [114b/306b is a stress relaxing layer],

the one or the plurality of fourth insulating films [111b/306b] has lower stress than the plurality of third insulating films [111b/306b is a stress relaxing layer],

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the plurality of first insulating films [114a/307a and 114c/307c] and the plurality of third insulating films [111a and 111c/306a and 306c] are inorganic insulating films [paragraph 0017],

the integrated circuit [104/303] provided over the substrate [112/302] is covered with the second adhesive [305],

the second adhesive [305] is in contact with the second sealing film [306], and

the second adhesive [305] is partly in contact with the substrate [302] over which the first adhesive [308], the first sealing film [307], and the integrated circuit [303] are provided [shown in fig.6B].

But Yamazaki does not disclose that the cover member [110] is sandwiched between the antenna and the second sealing films.

However, Yamazaki² [Fig.1] teaches a semiconductor component that has TFTs and antenna and cover member and it further teaches that the cover member [39] is sandwiched between the antenna [44] and the second sealing film [12].

Therefore it would have been obvious to one ordinary skill in the art at the time of the invention to place the cover member between the antenna and the second sealing film because with this structure the antenna would have contact to the outside and other circuits.

Yamazaki/Yamazaki² do not disclose that the integrated circuit and the antenna are electrically connected to each other via a contact hole formed in the cover member and the second sealing film with the second adhesive,

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Moon [Fig.7E] teaches that the integrated circuit [shown TFT] and the antenna [72] are electrically connected to each other via a contact hole [70] formed in the cover member [84] and the second sealing film [68] with the second adhesive [layer 68 is also adhesive see col.4, lines 21-40].

It is well known in the art to electrically connect an integrated circuit with an antenna by forming a contact hole in the cover member and the second sealing film with the second adhesive.

Therefore it would have been obvious to one ordinary skill in the art at the time of the invention to electrically connect an integrated circuit with an antenna by forming a contact hole in the cover member and the second sealing film with the second adhesive because this would make the antenna to be connected to the TFT and also to any circuit outside this package.

Regarding claim 8, Yamazaki in view of Yamazaki2 in view of Moon was discussed in claim 7. Yamazaki [paragraph 0077] teaches that the cover member [110] has flexibility.

Regarding claim 10, Yamazaki in view of Yamazaki2 in view of Moon was discussed in claim 7. Yamazaki [paragraph 0077] teaches that the substrate [112] has flexibility.

Regarding claim 11, Yamazaki in view of Yamazaki2 in view of Moon was discussed in claim 7. Yamazaki [paragraph 0070] teaches that the plurality of first insulating films [114a and 114c] or the plurality of third insulating films [111a and 111c] includes silicon nitride, silicon nitride oxide, aluminum oxide, aluminum nitride, aluminum nitride oxide or aluminum silicon nitride oxide.

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Regarding claim 12, Yamazaki in view of Yamazaki² in view of Moon was discussed in claim 7. Yamazaki [paragraph 0072] teaches that the one or the plurality of second insulating films [114b] or the one or the plurality of third insulating films [111b] includes polyimide, acrylic, polyamide, polyimide amide, benzocyclobutene or epoxy resin

Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Tanaka et al. (US 6,974,909 B2).

Regarding claim 9, Yamazaki [Figs.1-2B] teaches a semiconductor device comprising:

an integrated circuit using a thin film transistor [104a-c];

a first sealing film [114] ; a second sealing film [111]; an adhesive [113]; and a substrate [112],

wherein the integrated circuit [104] is sandwiched between the first sealing film [114] and the second sealing film [111], the first sealing film [114] is sandwiched between the substrate [112] and the integrated circuit [104].

the integrated circuit [104] includes a connection terminal [terminals are shown in Fig.1B but are not labeled],

the first sealing film [114] includes a plurality of first insulating films [114a and 114c] and one or a plurality of second insulating films [114b] sandwiched between the plurality of first insulating films [shown],

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the first sealing film [114/307] is attached to the substrate [112/302] with the adhesive [113/308 is a bonding layer that sticks the substrate and sealing film together as shown in fig.2B and 6B],

the second sealing film [111] includes a plurality of third insulating films [111a and 111c] and one or a plurality of fourth insulating films [111b] sandwiched between the plurality of third insulating films [shown],

the one or the plurality of second insulating films [114b] has lower stress than the plurality of first insulating films [114b is a stress relaxing layer],

the one or the plurality of fourth insulating films [111b] has lower stress than the plurality of third insulating films [111b is a stress relaxing layer], and

the plurality of first insulating films [114a and 114c] and the plurality of third insulating films [111a and 111c] are inorganic insulating films [paragraph 0017].

But Yamazaki does not disclose that the integrated circuit further includes a rectification circuit for generating a supply voltage from an alternating-current signal that is input in the connection terminal by an antenna;

a demodulation circuit for generating a first signal by demodulating the alternating-current signal; a microprocessor for performing arithmetic processing in accordance with the first signal to generate a second signal; a modulation circuit for modulating the second signal; and a switch for modulating load applied to the antenna in accordance with the modulated second signal.

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Tanaka [Fig. 7] teaches an integrated circuit that includes a rectification circuit [121] for generating a supply voltage from an alternating-current signal that is input in the connection terminal by an antenna [100];

a demodulation circuit [123] for generating a first signal by demodulating the alternating-current signal; a microprocessor [126] for performing arithmetic processing in accordance with the first signal to generate a second signal; a modulation circuit [circuit 20 that modulates a carrier wave] for modulating the second signal; and a switch for modulating load applied to the antenna in accordance with the modulated second signal [shown].

Therefore it would have been obvious to one ordinary skill in the art at the time of the invention to have associated the semiconductor component of Yamazaki with the circuit of Tanaka which includes rectifier, modulator/demodulator, microprocessor, and switch to control the voltage given to the TFTs by converting high voltage to low voltage and to make the semiconductor function.

Regarding claim 10, Yamazaki in view of Tanaka was discussed in claim 1-3. Yamazaki [paragraph 0077] teaches that the substrate [112] has flexibility.

Regarding claim 11, Yamazaki in view of Tanaka was discussed in claim 1-3. Yamazaki [paragraph 0070] teaches that the plurality of first insulating films [114a and 114c] or the plurality of third insulating films [111a and 111c] includes silicon nitride, silicon nitride oxide, aluminum oxide, aluminum nitride, aluminum nitride oxide or aluminum silicon nitride oxide.

Regarding claim 12, Yamazaki in view of Tanaka was discussed in claim 1-3. Yamazaki [paragraph 0072] teaches that the one or the plurality of second insulating films [114b] or the one

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or the plurality of third insulating films [111b] includes polyimide, acrylic, polyamide, polyimide amide, benzocyclobutene or epoxy resin

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HAJAR KOLAHDOUZAN whose telephone number is (571)270-5842. The examiner can normally be reached on Monday- Friday 7:30 A.M.- 5:00 P.M. EDT.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on (571) 272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HK

/Davienne Monbleau/
Supervisory Patent Examiner, Art Unit 2893